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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,469	12/20/2001	Eduardo Maayan	P-3454-US	3554

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EXAMINER	
NGUYEN, VIET Q	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,469	MAAYAN ET AL.	
	Examiner	Art Unit	
	Viet Q Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 6/9/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *17-23* is/are withdrawn from consideration.

5)☒ Claim(s) *1-14* is/are allowed.

6)☒ Claim(s) *15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/9/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-16 are present for examination per applicant's election.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim **16** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Takahashi (JP411354758A), and Iwahashi (JP0202001118392A), and Tsujikawa et al (JP409017981A), and Takumi et al (JP02002216488A), and Kotane et al (JP408106791A).**

All the references cited above obviously teach or at least show the following recited features:

- **Takahashi (see Fig.2)** shows a NOR array having a first plurality of cells each capable of storing at least one EEPROM bit (see Fig.3, detailed non-volatile memory cell structure), and a second plurality of select transistors (SB00 to SB51, Fig.10) as claimed select transistors each of which select a particular group (or a column) of one or more cells as similarly claimed;
- **Iwahashi (see Fig.14)** shows a NOR array (with plurality of bit lines, word lines, and common lines coupled to each cell's diffusion areas), and the array further having a first plurality of cells each capable of storing at least one EEPROM bit

(see Fig.28, detailed non-volatile memory cell structure), and a second plurality of select transistors (200s to 300s, Fig.14) as claimed select transistors each of which select a particular group (or a column) of one or more cells as similarly claimed;

- **Tsujikawa et al (see Fig.8)** shows a NOR array (with plurality of bit lines, word lines, and common lines coupled to the cell's diffusion areas), and the array further having a first plurality of cells (MC) each capable of storing at least one flash EEPROM bit (see solution description), and a second plurality of select transistors (N5 to N8, Fig.8) as claimed select transistors each of which select a particular group (or a column) of one or more cells as similarly claimed;
- **Takumi et al (see Fig.1)** shows a NOR array (with plurality of bit lines, word lines, and common lines coupled to the cell's diffusion areas), and the array further having a first plurality of cells, each capable of storing at least one flash EEPROM bit (see solution description), and a second plurality of select transistors (21 and 16, Fig.1) as claimed select transistors each of which select a particular group (or a column) of one or more cells as similarly claimed;
- **Kotane at al (see Fig. 1)** shows a NOR array (with plurality of bit lines, word lines, and common lines coupled to the cell's diffusion areas), and the array further having a first plurality of cells (T) each capable of storing at least one flash EEPROM bit (see solution description), and a second plurality of select transistors (ST1 to STn, Fig.1) as claimed select transistors each of which select a particular group (or a column) of one or more cells as similarly claimed.

It would have been obvious to one skilled in the art that at least one EEPROM bit can be stored in each memory cell structure from these above teachings.

3. Claim **15** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Eitan (6,429,063 B1).**

Eitan (see Fig. 3A) obviously shows a memory cell structure which capable of storing dual bits (one left and right sides) in each cell. Further, it would be obvious to one skilled in this art that such cell could be configured to store both EEPROM bit as well as Flash EEPROM bit since Eitan has suggested the FLASH memory technology in the field of the invention.

4. Other claims contain allowable subject matter over prior arts of record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V. Nguyen
7/8/2004

Viet Q Nguyen
Primary Examiner
Art Unit 2818